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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/663,690	09/19/2000	Hiroki Kanno	016907/1147	5295

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2626	

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/663,690	Applicant(s) KANNO ET AL.	
	Examiner Melanie M Vida	Art Unit 2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

JEROME GRANT II
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement(s) (IDS) submitted on 1/23/03 has been considered by the examiner and is attached to this office action.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: Apparatus for M-bit, Multi-level Image Conversion using Weighted Error Diffusion.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a) because they fail to show in figures 2-6 and 8-9, 11-12, 15, 19-32, the English language equivalent for each of the components, as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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5. **Claim 1, 4-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Takaoka et al. US-PAT-NO: 5,162,925 (hereinafter, Takaoka), and further in view of Rombola et al. US-PAT-NO: 5,689,588, (hereinafter, Rombola).

Regarding, **claim 1,** Takaoka, as shown in figure 10, teaches a circuit construction processing, which reads on "an image processing circuit", (col. 3, lines 51-53). Bit discarding circuits (10 and 12), which reads on "a first processing circuit", and a masking circuit (13'), which reads on "and a second processing circuit" are connected in 6 bits, which reads on "are connected in m bits", (col. 7, lines 4-13). Takaoka teaches of a bit discarding circuits (10 and 12) and a masking circuit (13'), which reads on "replacement means" for extracting the two least significant bits, and replacing the 6 bit data to 8-bit data by the masking table which uses equation 1, which reads on "for replacing lower n bits of an m bit image signal with n-bit additional information, and outputting an m-bit conversion image signal", (col. 5, lines 56-61). The subtractor (24), which reads on "error calculation means", calculates an 8-bit M_o signal, which reads on "for calculating an error", (col. 8, lines 57-60). This error represents a difference between an 8-bit signal output from the masking table, which reads on "for calculating an error between the m-bit conversion image signal replaced by the replacement means", and the 8-bit output signal from LUT (22), which reads on "and the m-bit image signal before the replacement", (col. 6, lines 64 through col. 7, lines 3). Further, a FIFO circuits (16-0) to (16-n), which reads on "error buffer" stores the diffusion data, which reads on "for storing the error calculated by the error calculation means", (col. 4, lines 60-61). The matrix showing the

weighting coefficients are to be multiplied with the latch data, which reads on "weight coefficient storage means for prestoring a weight coefficient for calculating a weight error", (col. 4, lines 17-21). The latching circuit (14), which reads on "weight error calculation means" are weighted with some of the errors of the surrounding picture elements and the 8-bits of data considered as reducing the accuracy at the time of the reduction in the number of bits are calculated, which reads on "for correcting the m-bit image signal before replacement, using the weight error calculated by the weight error calculation means", (col. 4, lines 63-67).

Takaoka does not expressly disclose, "error correction means" or "extraction means".

However, Rombola, as shown in figure 1a, teaches of obtaining a modified density value (30) based on a current pixel density value (20) and an error diffused (40), which reads on "error correction means for correcting the m-bit image signal before the replacement", (col. 3, lines 33-38; col. 4, lines 10-20). Rombola states that the errors are weighted by multiplying each by a suitable coefficient so that errors in pixels closer to pixel X have more of an affect on adjustments to modify pixel X, which reads on "using the weight error calculated by the weight error calculation means;" (col. 4, lines 5-10). Additionally, Rombola teaches that based on the rendered pixel value output from a gray level thresholding (50), the LSB (i.e. least significant bit) is extracted from the MSB (most significant bit), which reads on "extraction means for extracting the lower n bits of the m-bit conversion image signal replaced and output from the replacement means", (col. 4, lines 30-38).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka's color image processor with Rombola's image processing apparatus.

One of ordinary skill in the art would have been motivated to use Rombola's image processing apparatus with Takaoka's color image processor, because both have bit discarding in order to correct for the upper M bits in the N bits of a digital color image signal, given the express suggestion of Takaoka, (col. 1, lines 60-66).

Regarding, **claim 2,** Takaoka, as shown in figure 5, that the **Y** (ie. yellow), **M** (i.e. Magenta), and **C** (i.e. Cyan) are color separated prior to discarding bits, which reads on "the m-bit conversion image signal is only a specific color component of color-separated color image signals", (col. 3, lines 35-45).

Regarding, **claim 4,** Takaoka, as shown in figure 10, teaches a circuit construction processing, which reads on "an image processing circuit", (col. 3, lines 51-53). Bit discarding circuits (10 and 12), which reads on "a first processing circuit", and a masking circuit (13'), which reads on "and a second processing circuit" are connected in 6 bits, which reads on "are connected in m bits", (col. 7, lines 4-13). As shown in figure 10, a block diagram processes separated color signals, Y, M and C each comprised of 8-bits, which reads on "a multi-value means for subjecting an m-bit image signal", (col. 6, lines 41-44). Further, the block diagram subjects these separated color image signals, Y, and C, to a bit discarding circuit, to discard the 2 lower-order bits to convert 8 bit to 6-bits, which reads on "for subjecting an m-bit image signal to a multi-value process and converting the m-bit image signal to m-n bit image signal", (col. 5, lines 57-63).

The subtractor (24), which reads on "error calculation means", calculates an 8-bit M_o signal, which reads on "for calculating an error", (col. 8, lines 57-60). This error represents a

difference between an 8-bit signal output from the masking table, which reads on "for calculating an error between the m-nbit conversion image signal multi-value-processed by the multi-value means", and the 8-bit output signal from LUT (22), which reads on "and the m-bit image signal subjected to the multi-value process;" (col. 6, lines 64 through col. 7, lines 3).

Further, a FIFO circuits (16-0) to (16-n), which reads on "error buffer" stores the diffusion data, which reads on "for storing the error calculated by the error calculation means", (col. 4, lines 60-61).

The matrix showing the weighting coefficients are to be multiplied with the latch data, which reads on "weight coefficient storage means for prestoring a weight coefficient for calculating a weight error", (col. 4, lines 17-21).

The latching circuit (14), which reads on "weight error calculation means" are weighted with some of the errors of the surrounding picture elements and the 8-bits of data considered as reducing the accuracy at the time of the reduction in the number of bits are calculated, which reads on "for calculating the weight error by multiplying the error stored in the error buffer by the weight coefficient stored in the weight coefficient storage means;", (col. 4, lines 63-67).

Takaoka does not expressly disclose, "error correction means", "addition means", "a first extraction means", or a "second extraction means".

However, Rombola, as shown in figure 1a, teaches of obtaining a modified density value (30) based on a current pixel density value (20) and an error diffused (40), which reads on "error correction means for correcting the m-bit image signal before the multi-value process", (col. 3, lines 33-38; col. 4, lines 10-20).

Rombola states that the errors are weighted by multiplying each by a suitable coefficient so that errors in pixels closer to pixel X have more of an affect on adjustments to modify pixel X, which reads on "using the weight error calculated by the weight error calculation means;" (col. 4, lines 5-10).

Rombola teaches of a uniformity corrector (110), as shown in figure 1a, which reads on "addition means" that stitches together the two bit planes (i.e. MSB signal and a LSB signal) and outputs a signal to a print head, which reads on "for adding n-bit information to m-n bit image signal multi-valued processed by the multi-value means, and outputting an m-bit conversion image signal", (col. 4, lines 49-53).

Additionally, Rombola inherently teaches the "first extraction means", and the second extraction means" as evidenced in the separation of the LSB (i.e. least significant bit) and the MSB (most significant bit) among a rendered pixel value output from a gray level thresholding (50), the LSB (i.e. least significant bit) is extracted from the MSB (most significant bit), which reads on "for extracting information bits of n bits from the m-bit conversion image signal output from the addition means", and "for extracting image bits of m-n bits from the m-bit conversion image signal output from the addition means", (col. 4, lines 30-38).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka's color image processor with Rombola's image processing apparatus.

One of ordinary skill in the art would have been motivated to use Rombola's image processing apparatus with Takaoka's color image processor, because both have bit discarding in

order to correct for the upper M bits in the N bits of a digital color image signal, given the express suggestion of Takaoka, (col. 1, lines 60-66).

Regarding, **claim 5,** Takaoka, as shown in figure 10, teaches a circuit construction processing, which reads on "an image processing circuit", (col. 3, lines 51-53). Bit discarding circuits (10 and 12), which reads on "a first processing circuit", and a masking circuit (13'), which reads on "and a second processing circuit" are connected in 6 bits, which reads on "are connected in m bits", (col. 7, lines 4-13). Takaoka inherently teaches "first replacement information pixel determination means for specifying n pixels within j x k pixels", as evidenced by figure 10, the circuit construction processing the color masking on the M component in the range of the input of Y, M, and C, as shown in figure 10, (col. 6, lines 43-44).

Further, the block diagram in figure 10, which reads on "replacement means" subjects these separated color image signals, Y, and C, to a bit discarding circuit, to discard the 2 lower-order bits to convert 8 bit to 6-bits, which reads on "for replacing, where the first replacement information pixel determination means has determined that process target pixels are specific n pixels, specific bits of an m-bit image signal", (col. 5, lines 57-63). Additionally, the color masking circuit (13') adds specific bits to the 6-bit signal to acquire an 8-bit signal, which reads on "with specific bits of n-bit additional information, and outputting an m-bit conversion image signal" (col. 5, lines 57-63).

Takaoka does not expressly disclose "second replacement information pixel determination means", or "information bit extraction means".

However, Rombola teaches a document scanner outputs a current pixel density value that is modified by an error diffusion process, and subsequently replaced with a rendered pixel value,

via a grey level thresholding, which reads on "second replacement information pixel determination means for specifying n pixels within j x k pixels;" (col. 4, lines 1-20). At block (60), as shown in figure 1a, the rendered pixel value is subjected to bit plane separation comprised of two planes, the LSB plane, and the MSB plane, which reads on "information bit extraction means for extracting, where the second replacement information pixel determination means has determined that process target pixels are specific n pixels, specific bits of the m-bit conversion signal output from the replacements means", (col. 4, lines 30-35). Through compression, expansion, and uniformity correction (110), the bit planes are stitched together, and sent to a print head (120), which reads on "and reconstructing information bits of n bits within the j x k pixels", (col. 4, lines 36-53).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka's first replacement means, with Rombola's second replacement means.

One of ordinary skill in the art would have been motivated to have a second replacement means, in order to detect a pattern of bits that have been processed, given the express suggestion of Rombola, (col. 2, lines 9-12).

Regarding, **claim 6,** Takaoka, as shown in figure 10, teaches a circuit construction processing, which reads on "an image processing circuit", (col. 3, lines 51-53). Bit discarding circuits (10 and 12), which reads on "a first processing circuit", and a masking circuit (13'), which reads on "and a second processing circuit" are connected in 6 bits, which reads on "are connected in m bits", (col. 7, lines 4-13). Takaoka inherently teaches "first replacement information pixel determination means for specifying n pixels within j x k pixels", as evidenced

by figure 10, the circuit construction processing the color masking on the M component in the range of the input of Y, M, and C, as shown in figure 10, (col. 6, lines 43-44).

Further, the block diagram in figure 10, which reads on "replacement means" subjects these separated color image signals, Y, and C, to a bit discarding circuit, to discard the 2 lower-order bits to convert 8 bit to 6-bits, which reads on "for replacing, where the first replacement information pixel determination means has determined that process target pixels are specific n pixels, specific bits of an m-bit image signal", (col. 5, lines 57-63). Additionally, the color masking circuit (13') adds specific bits to the 6-bit signal to acquire an 8-bit signal, which reads on "with specific bits of n-bit additional information, and outputting an m-bit conversion image signal" (col. 5, lines 57-63).

The subtractor (24), which reads on "error calculation means", calculates an 8-bit M_o signal, which reads on "for calculating an error", (col. 8, lines 57-60). This error represents a difference between an 8-bit signal output from the masking table, which reads on "for calculating an error between the m-bit conversion image signal replaced by the replacement means", and the 8-bit output signal from LUT (22), which reads on "and the m-bit image signal before the replacement", (col. 6, lines 64 through col. 7, lines 3). Further, a FIFO circuits (16-0) to (16-n), which reads on "error buffer" stores the diffusion data, which reads on "for storing the error calculated by the error calculation means", (col. 4, lines 60-61). The matrix showing the weighting coefficients are to be multiplied with the latch data, which reads on "weight coefficient storage means for prestoring a weight coefficient for calculating a weight error", (col. 4, lines 17-21). The latching circuit (14), which reads on "weight error calculation means" are weighted with some of the errors of the surrounding picture elements and the 8-bits of data

considered as reducing the accuracy at the time of the reduction in the number of bits are calculated, which reads on "for correcting the m-bit image signal before replacement, using the weight error calculated by the weight error calculation means", (col. 4, lines 63-67).

Takaoka does not expressly disclose, "error correction means", "second replacement information pixel determination means", or "information bit extraction means".

However, Rombola, as shown in figure 1a, teaches of obtaining a modified density value (30) based on a current pixel density value (20) and an error diffused (40), which reads on "error correction means for correcting the m-bit image signal before the replacement", (col. 3, lines 33-38; col. 4, lines 10-20). Rombola states that the errors are weighted by multiplying each by a suitable coefficient so that errors in pixels closer to pixel X have more of an affect on adjustments to modify pixel X, which reads on "using the weight error calculated by the weight error calculation means;" (col. 4, lines 5-10).

Rombola teaches a document scanner outputs a current pixel density value that is modified by an error diffusion process, and subsequently replaced with a rendered pixel value, via a grey level thresholding, which reads on "second replacement information pixel determination means for specifying n pixels within j x k pixels;" (col. 4, lines 1-20). At block (60), as shown in figure 1a, the rendered pixel value is subjected to bit plane separation comprised of two planes, the LSB plane, and the MSB plane, which reads on "information bit extraction means for extracting, where the second replacement information pixel determination means has determined that process target pixels are specific n pixels, specific bits of the m-bit conversion signal output from the replacements means", (col. 4, lines 30-35). Through compression, expansion, and uniformity correction (110), the bit planes are stitched together, and

sent to a print head (120), which reads on "and reconstructing information bits of n bits within the j x k pixels", (col. 4, lines 36-53).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka's color image processor with Rombola's image processing apparatus.

One of ordinary skill in the art would have been motivated to use Rombola's image processing apparatus with Takaoka's color image processor, because both have bit discarding in order to correct for the upper M bits in the N bits of a digital color image signal, given the express suggestion of Takaoka, (col. 1, lines 60-66).

Regarding, **claim 7,** Takaoka, as shown in figure 10, teaches a circuit construction processing, which reads on "an image processing circuit", (col. 3, lines 51-53). Bit discarding circuits (10 and 12), which reads on "a first processing circuit", and a masking circuit (13'), which reads on "and a second processing circuit" are connected in 6 bits, which reads on "are connected in m bits", (col. 7, lines 4-13). Takaoka inherently teaches "first replacement information pixel determination means for specifying n pixels within j x k pixels", as evidenced by figure 10, the circuit construction processing the color masking on the M component in the range of the input of Y, M, and C, as shown in figure 10, (col. 6, lines 43-44).

Further, the block diagram in figure 10, which reads on "replacement means" subjects these separated color image signals, Y, and C, to a bit discarding circuit, to discard the 2 lower-order bits to convert 8 bit to 6-bits, which reads on "for replacing, where the first replacement information pixel determination means has determined that process target pixels are specific n

pixels, specific bits of an m-bit image signal", (col. 5, lines 57-63). Additionally, the color masking circuit (13') adds specific bits to the 6-bit signal to acquire an 8-bit signal, which reads on "with specific bits of n-bit additional information, and outputting an m-bit conversion image signal" (col. 5, lines 57-63).

The subtractor (24), which reads on "error calculation means", calculates an 8-bit M_o signal, which reads on "for calculating an error", (col. 8, lines 57-60). This error represents a difference between an 8-bit signal output from the masking table, which reads on "for calculating an error between the m-bit conversion image signal replaced by the replacement means", and the 8-bit output signal from LUT (22), which reads on "and the m-bit image signal before the replacement", (col. 6, lines 64 through col. 7, lines 3). Further, a FIFO circuits (16-0) to (16-n), which reads on "error buffer" stores the diffusion data, which reads on "for storing the error calculated by the error calculation means", (col. 4, lines 60-61). The matrix showing the weighting coefficients are to be multiplied with the latch data, which reads on "weight coefficient storage means for prestoring a weight coefficient for calculating a weight error", (col. 4, lines 17-21). The latching circuit (14), which reads on "weight error calculation means" are weighted with some of the errors of the surrounding picture elements and the 8-bits of data considered as reducing the accuracy at the time of the reduction in the number of bits are calculated, which reads on "for correcting the m-bit image signal before replacement, using the weight error calculated by the weight error calculation means", (col. 4, lines 63-67).

Takaoka does not expressly disclose, "error correction means", "second replacement information pixel determination means", or "extraction means".

However, Rombola, as shown in figure 1a, teaches of obtaining a modified density value (30) based on a current pixel density value (20) and an error diffused (40), which reads on "error correction means for correcting the m-bit image signal before the replacement", (col. 3, lines 33-38; col. 4, lines 10-20). Rombola states that the errors are weighted by multiplying each by a suitable coefficient so that errors in pixels closer to pixel X have more of an affect on adjustments to modify pixel X, which reads on "using the weight error calculated by the weight error calculation means;" (col. 4, lines 5-10).

Rombola teaches a document scanner outputs a current pixel density value that is modified by an error diffusion process, and subsequently replaced with a rendered pixel value, via a grey level thresholding, which reads on "second replacement information pixel determination means for specifying n pixels within j x k pixels;" (col. 4, lines 1-20).

Additionally, Rombola teaches that based on the rendered pixel value output from a gray level thresholding (50), the LSB (i.e. least significant bit) is extracted from the MSB (most significant bit), which reads on "extraction means for extracting the lower n bits of the m-bit conversion image signal replaced and output from the replacement means", (col. 4, lines 30-38).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka's color image processor with Rombola's image processing apparatus.

One of ordinary skill in the art would have been motivated to use Rombola's image processing apparatus with Takaoka's color image processor, because both have bit discarding in order to correct for the upper M bits in the N bits of a digital color image signal, given the express suggestion of Takaoka, (col. 1, lines 60-66).

Regarding, **claim 8,** Takaoka, as shown in figure 10, teaches a circuit construction processing, which reads on "an image processing circuit", (col. 3, lines 51-53). Bit discarding circuits (10 and 12), which reads on "a first processing circuit", and a masking circuit (13'), which reads on "and a second processing circuit" are connected in 6 bits, which reads on "are connected in m bits", (col. 7, lines 4-13). As shown in figure 10, a block diagram processes separated color signals, Y, M and C comprised of 8-bits per signal, as shown, which reads on "a multi-value means for subjecting an m-bit image signal", (col. 6, lines 41-44). Further, the block diagram subjects these separated color image signals, Y, and C, to a bit discarding circuit, to discard the 2 lower-order bits of the 8 bit image signal to obtain a 6-bit color image signal, which reads on "for subjecting an m-bit image signal to a multi-value process and converting the m-bit image signal to 1-n ($n < 1 < m$) bit image signal;" (col. 5, lines 57-63). The subtractor (24), which reads on "error calculation means", calculates an 8-bit M_o signal, which reads on "for calculating an error", (col. 8, lines 57-60). This error represents a difference between an 8-bit signal output from the masking table, which reads on "for calculating an error between the m-nbit conversion image signal multi-value-processed by the multi-value means", and the 8-bit output signal from LUT (22), which reads on "and the m-bit image signal subjected to the multi-value process;" (col. 6, lines 64 through col. 7, lines 3).

Further, a FIFO circuits (16-0) to (16-n), which reads on "error buffer" stores the diffusion data, which reads on "for storing the error calculated by the error calculation means", (col. 4, lines 60-61).

The matrix showing the weighting coefficients are to be multiplied with the latch data, which reads on "weight coefficient storage means for prestoring a weight coefficient for calculating a weight error", (col. 4, lines 17-21).

The latching circuit (14), which reads on "weight error calculation means" are weighted with some of the errors of the surrounding picture elements and the 8-bits of data considered as reducing the accuracy at the time of the reduction in the number of bits are calculated, which reads on "for calculating the weight error by multiplying the error stored in the error buffer by the weight coefficient stored in the weight coefficient storage means;", (col. 4, lines 63-67).

Takaoka does not expressly disclose, "error correction means", "addition means", "a first extraction means", or a "second extraction means".

However, Rombola, as shown in figure 1a, teaches of obtaining a modified density value (30) based on a current pixel density value (20) and an error diffused (40), which reads on "error correction means for correcting the m-bit image signal before the multi-value process", (col. 3, lines 33-38; col. 4, lines 10-20).

Rombola states that the errors are weighted by multiplying each by a suitable coefficient so that errors in pixels closer to pixel X have more of an affect on adjustments to modify pixel X, which reads on "using the weight error calculated by the weight error calculation means;" (col. 4, lines 5-10).

Rombola teaches of a uniformity corrector (110), as shown in figure 1a, which reads on "addition means" that stitches together the two bit planes (i.e. MSB signal and a LSB signal) and outputs a signal to a print head, which reads on "for adding n-bit information to 1-n bit image

signal multi-valued processed by the multi-value means, and outputting an 1-bit conversion image signal", (col. 4, lines 49-53).

Additionally, Rombola inherently teaches the "first extraction means", and the second extraction means" as evidenced in the separation of the LSB (i.e. least significant bit) and the MSB (most significant bit) among a rendered pixel value output from a gray level thresholding (50), the LSB (i.e. least significant bit) is extracted from the MSB (most significant bit), which reads on "for extracting information bits of n bits from the m-bit conversion image signal output from the addition means", and "for extracting image bits of m-n bits from the m-bit conversion image signal output from the addition means", (col. 4, lines 30-38).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka's color image processor with Rombola's image processing apparatus.

One of ordinary skill in the art would have been motivated to use Rombola's image processing apparatus with Takaoka's color image processor, because both have bit discarding in order to correct for the upper M bits in the N bits of a digital color image signal, given the express suggestion of Takaoka, (col. 1, lines 60-66).

Regarding, **claim 9,** Takaoka, as shown in figure 10, teaches a circuit construction processing, which reads on "an image processing circuit", (col. 3, lines 51-53). Bit discarding circuits (10 and 12), which reads on "a first processing circuit", and a masking circuit (13'), which reads on "and a second processing circuit" are connected in 6 bits, which reads on "are connected in m bits", (col. 7, lines 4-13).

Takaoka does not expressly disclose, a "multi-value dithering means for subjecting an m-bit image signal to a multi-value process and converting the m-bit image signal to an m-n bit image signal", "addition means", "first extraction means" or a "second extraction means".

However, Rombola teaches of a gray level thresholding that is applied to a modified density value, which reads on "a multi-value dithering means for subjecting an m-bit image signal to a multi-value process", (col. 4, lines 31-37). Furthermore, Rombola teaches of separately compressing the LSB (i.e. the least significant bit) and the MSB (i.e. most significant bits), which reads on "and converting the m-bit image signal to an m-n bit image signal", (col. 4, lines 31-37).

Rombola teaches of a uniformity corrector (110), as shown in figure 1a, which reads on "addition means" that stitches together the two bit planes (i.e. MSB signal and a LSB signal) and outputs a signal to a print head, which reads on "for adding n-bit information to 1-n bit image signal multi-valued processed by the multi-value means, and outputting an 1-bit conversion image signal", (col. 4, lines 49-53).

Additionally, Rombola inherently teaches the "first extraction means", and the second extraction means" as evidenced in the separation of the LSB (i.e. least significant bit) and the MSB (most significant bit) among a rendered pixel value output from a gray level thresholding (50), the LSB (i.e. least significant bit) is extracted from the MSB (most significant bit), which reads on "for extracting information bits of n bits from the m-bit conversion image signal output

from the addition means", and "for extracting image bits of m-n bits from the m-bit conversion image signal output from the addition means", (col. 4, lines 30-38).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka's circuit with Rombola's multi-value dithering means and m-bit image signal conversion to a m-n bit image signal.

One of ordinary skill in the art would have been motivated to separate an m-bit multi-valued dithered signal to an m-n bit image signal because the LSB of a multi-bit error diffused image tends to compress poorly, given the express suggestion of Rombola, (col. 1, lines 53-54).

Regarding, **claim 10,** Takaoka, as shown in figure 10, teaches a circuit construction processing, which reads on "an image processing circuit", (col. 3, lines 51-53). Bit discarding circuits (10 and 12), which reads on "a first processing circuit", and a masking circuit (13'), which reads on "and a second processing circuit" are connected in 6 bits, which reads on "are connected in m bits", (col. 7, lines 4-13).

Takaoka inherently teaches, "difference information extraction means for extracting a difference of n-bit additional information of successive two pixels" as evidenced by a shift circuit (18) as shown in figure 6, that shifts the two lower bits to create a 6-bit signal from a 8-bit signal, (col. 4, lines 5-10).

Takaoka teaches of a bit discarding circuits (10 and 12) and a masking circuit (13'), which reads on "replacement means" for extracting the two least significant bits, and replacing the 6 bit data to 8-bit data by the masking table which uses equation 1, which reads on "for replacing where the difference extracted by the difference information extraction means is not 0,

n bits from lower n+1 bits of an m-bit image signal with additional information, a least significant bit with 1, and also replacing where the difference extracted by the difference information extraction means is 0, the least significant bit with 0, and outputting an m-bit conversion image signal", (col. 5, lines 56-61).

The subtractor (24), which reads on "error calculation means", calculates an 8-bit M_o signal, which reads on "for calculating an error", (col. 8, lines 57-60). This error represents a difference between an 8-bit signal output from the masking table, which reads on "for calculating an error between the m-bit conversion image signal replaced by the replacement means", and the 8-bit output signal from LUT (22), which reads on "and the m-bit image signal before the replacement", (col. 6, lines 64 through col. 7, lines 3). Further, a FIFO circuits (16-0) to (16-n), which reads on "error buffer" stores the diffusion data, which reads on "for storing the error calculated by the error calculation means", (col. 4, lines 60-61). The matrix showing the weighting coefficients are to be multiplied with the latch data, which reads on "weight coefficient storage means for prestoring a weight coefficient for calculating a weight error", (col. 4, lines 17-21). The latching circuit (14), which reads on "weight error calculation means" are weighted with some of the errors of the surrounding picture elements and the 8-bits of data considered as reducing the accuracy at the time of the reduction in the number of bits are calculated, which reads on "for correcting the m-bit image signal before replacement, using the weight error calculated by the weight error calculation means", (col. 4, lines 63-67).

Takaoka does not expressly disclose, "error correction means" or "extraction means".

However, Rombola, as shown in figure 1a, teaches of obtaining a modified density value (30) based on a current pixel density value (20) and an error diffused (40), which reads on "error

correction means for correcting the m-bit image signal before the replacement", (col. 3, lines 33-38; col. 4, lines 10-20). Rombola states that the errors are weighted by multiplying each by a suitable coefficient so that errors in pixels closer to pixel X have more of an affect on adjustments to modify pixel X, which reads on "using the weight error calculated by the weight error calculation means;" (col. 4, lines 5-10). Additionally, Rombola teaches that based on the rendered pixel value output from a gray level thresholding (50), the LSB (i.e. least significant bit) is extracted from the MSB (most significant bit), which reads on "extraction means for extracting the lower n bits of the m-bit conversion image signal replaced and output from the replacement means", (col. 4, lines 30-38).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka's color image processor with Rombola's image processing apparatus.

One of ordinary skill in the art would have been motivated to use Rombola's image processing apparatus with Takaoka's color image processor, because both have bit discarding in order to correct for the upper M bits in the N bits of a digital color image signal, given the express suggestion of Takaoka, (col. 1, lines 60-66).

Regarding, **claim 11,** Takaoka, as shown in figure 10, teaches a circuit construction processing, which reads on "an image processing circuit", (col. 3, lines 51-53). Bit discarding circuits (10 and 12), which reads on "a first processing circuit", and a masking circuit (13'), which reads on "and a second processing circuit" are connected in 6 bits, which reads on "are connected in m bits", (col. 7, lines 4-13).

Takaoka inherently teaches "first replacement information pixel determination means for specifying n pixels within j x k pixels", as evidenced by figure 10, the circuit construction processing the color masking on the M component in the range of the input of Y, M, and C, as shown in figure 10, (col. 6, lines 43-44).

Further, the block diagram in figure 10, which reads on "replacement means" subjects these separated color image signals, Y, and C, to a bit discarding circuit, to discard the 2 lower-order bits to convert 8 bit to 6-bits, which reads on "for replacing, where the first replacement information pixel determination means has determined that process target pixels are specific n pixels, specific bits of an m-bit image signal", (col. 5, lines 57-63). Additionally, the color masking circuit (13') adds specific bits to the 6-bit signal to acquire an 8-bit signal, which reads on "with specific bits of n-bit additional information, and outputting an m-bit conversion image signal" (col. 5, lines 57-63).

The subtractor (24), which reads on "error calculation means", calculates an 8-bit M_o signal, which reads on "for calculating an error", (col. 8, lines 57-60). This error represents a difference between an 8-bit signal output from the masking table, which reads on "for calculating an error between the m-bit conversion image signal replaced by the replacement means", and the 8-bit output signal from LUT (22), which reads on "and the m-bit image signal before the replacement", (col. 6, lines 64 through col. 7, lines 3). Further, a FIFO circuits (16-0) to (16-n), which reads on "error buffer" stores the diffusion data, which reads on "for storing the error calculated by the error calculation means", (col. 4, lines 60-61). The matrix showing the weighting coefficients are to be multiplied with the latch data, which reads on "weight coefficient storage means for prestoring a weight coefficient for calculating a weight error", (col.

4, lines 17-21). The latching circuit (14), which reads on "weight error calculation means" are weighted with some of the errors of the surrounding picture elements and the 8-bits of data considered as reducing the accuracy at the time of the reduction in the number of bits are calculated, which reads on "for correcting the m-bit image signal before replacement, using the weight error calculated by the weight error calculation means", (col. 4, lines 63-67).

Takaoka does not expressly disclose, "error correction means", "second replacement information pixel determination means", or "extraction means".

However, Rombola, as shown in figure 1a, teaches of obtaining a modified density value (30) based on a current pixel density value (20) and an error diffused (40), which reads on "error correction means for correcting the m-bit image signal before the replacement", (col. 3, lines 33-38; col. 4, lines 10-20). Rombola states that the errors are weighted by multiplying each by a suitable coefficient so that errors in pixels closer to pixel X have more of an affect on adjustments to modify pixel X, which reads on "using the weight error calculated by the weight error calculation means;" (col. 4, lines 5-10).

Rombola teaches a document scanner outputs a current pixel density value that is modified by an error diffusion process, and subsequently replaced with a rendered pixel value, via a grey level thresholding, which reads on "second replacement information pixel determination means for specifying n pixels within j x k pixels;" (col. 4, lines 1-20).

Additionally, Rombola teaches that based on the rendered pixel value output from a gray level thresholding (50), the LSB (i.e. least significant bit) is extracted from the MSB (most significant bit), which reads on "extraction means for extracting the lower n bits of the m-bit conversion image signal replaced and output from the replacement means", (col. 4, lines 30-38).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka's color image processor with Rombola's image processing apparatus.

One of ordinary skill in the art would have been motivated to use Rombola's image processing apparatus with Takaoka's color image processor, because both have bit discarding in order to correct for the upper M bits in the N bits of a digital color image signal, given the express suggestion of Takaoka, (col. 1, lines 60-66).

Regarding, **claim 12,** Takaoka, as shown in figure 10, teaches a circuit construction processing, which reads on "an image processing circuit", (col. 3, lines 51-53). Bit discarding circuits (10 and 12), which reads on "a first processing circuit", and a masking circuit (13'), which reads on "and a second processing circuit" are connected in 6 bits, which reads on "are connected in m bits", (col. 7, lines 4-13).

6. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Takaoka et al. US-PAT-NO: 5,162,925 (hereinafter, Takaoka), and further in view of Rombola et al. US-PAT-NO: 5,689,588, (hereinafter, Rombola) as applied to claim 1 above, and further in view of Suzuki et al. US-PAT-NO: 5,907,370, (hereinafter, Suzuki).

Regarding, **claim 3,** Takaoka in view of Rombola teach the image processing apparatus of claim 1, but fail to expressly disclose, "wherein the m-bit image signal before replacement is a color difference component of a color image signal represented by a luminance and a color difference".

However, Suzuki, as shown in figure 15, teaches a preprocessing circuit (Y/C separation), for an input video signal (10) that is composed of a luminance signal and a color difference signal, which reads on "the m-bit image signal before the replacement is a color difference component of a color image signal represented by a luminance and a color difference", (col. 11, lines 1-4).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka in view of Rombola's image processing apparatus (i.e. claim 1) with Suzuki's luminance signal and a color difference signal representing a video input signal (VD).

One of ordinary skill in the art would have been motivated to represent the m-bit image signal before replacement with a color difference component and a luminance, in order to process them in parallel and distinctly, given the express suggestion of Suzuki, (col. 12, lines 9-16).

7. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Takaoka et al. US-PAT-NO: 5,162,925 (hereinafter, Takaoka) in view of Suzuki et al. US-PAT-NO: 5,907,370, (hereinafter, Suzuki) and further in view of Rombola et al. US-PAT-NO: 5,689,588, (hereinafter, Rombola)

Regarding, **claim 12,** Takaoka, as shown in figure 10, teaches a circuit construction processing, which reads on "an image processing circuit", (col. 3, lines 51-53). Bit discarding circuits (10 and 12), which reads on "a first processing circuit", and a masking circuit (13'), which reads on "and a second processing circuit" are connected in 6 bits, which reads on "are connected in m bits", (col. 7, lines 4-13).

The subtractor (24), which reads on "error calculation means", calculates an 8-bit M_o signal, which reads on "for calculating an error", (col. 8, lines 57-60). This error represents a difference between an 8-bit signal output from the masking table, which reads on "for calculating an error between the m-bit conversion image signal replaced by the replacement means", and the 8-bit output signal from LUT (22), which reads on "and the m-bit image signal before the replacement", (col. 6, lines 64 through col. 7, lines 3). Further, a FIFO circuits (16-0) to (16-n), which reads on "error buffer" stores the diffusion data, which reads on "for storing the error calculated by the error calculation means", (col. 4, lines 60-61). The matrix showing the weighting coefficients are to be multiplied with the latch data, which reads on "weight coefficient storage means for prestoring a weight coefficient for calculating a weight error", (col. 4, lines 17-21). The latching circuit (14), which reads on "weight error calculation means" are weighted with some of the errors of the surrounding picture elements and the 8-bits of data considered as reducing the accuracy at the time of the reduction in the number of bits are calculated, which reads on "for correcting the m-bit image signal before replacement, using the weight error calculated by the weight error calculation means", (col. 4, lines 63-67).

Takaoka does not teach the conversion means or the replacement means.

However, Suzuki teaches that an n-bit image signal is expanded by adding to a LSB (least significant bit) a "0" to perform bit expansion, which reads on "conversion means for converting n-bit additional information to a random n-bit string", (col. 5, lines 49-59). A 10-bit expanding circuit transfers the output signal (S2) to a control signal based on the type of image signal for converting the signal in a converting unit (130) into an m-bit signal in response to a control signal, which reads on "replacement means for replacing lower n bits of an m-bit image signal

with the random n-bit spring converted by the conversion means, and outputting an m-bit conversion image signal", (col. 5, lines 60-67).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka image processing apparatus with Suzuki's 10-bit expanding circuit and converting unit (130).

One of ordinary skill in the art would have been motivated to represent the m-bit image signal before replacement with a random n-bit string in order to prevent any artifacts or moiré.

Takaoka in view of Suzuki do not expressly disclose, "error correction means", or the "extraction means", or the "inverse conversion means".
However, Rombola, as shown in figure 1a, teaches of obtaining a modified density value (30) based on a current pixel density value (20) and an error diffused (40), which reads on "error correction means for correcting the m-bit image signal before the replacement", (col. 3, lines 33-38; col. 4, lines 10-20). Rombola states that the errors are weighted by multiplying each by a suitable coefficient so that errors in pixels closer to pixel X have more of an affect on adjustments to modify pixel X, which reads on "using the weight error calculated by the weight error calculation means;" (col. 4, lines 5-10). Additionally, Rombola teaches that based on the rendered pixel value output from a gray level thresholding (50), the LSB (i.e. least significant bit) is extracted from the MSB (most significant bit), which reads on "extraction means for extracting the lower n bits of the m-bit conversion image signal replaced and output from the replacement means", (col. 4, lines 30-38).

Further, Rombola teaches that the uniformity correction (110) stitches together the two bit planes, which reads on "inverse conversion means for subjecting the lower n bits extracted by

the extraction means to an inverse conversion of the conversion by the conversion means", (col. 4, lines 50-53).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Takaoka's in view of Suzuki's color image processor with Rombola's image processing apparatus.

One of ordinary skill in the art would have been motivated to use Rombola's image processing apparatus with Takaoka in view of Suzuki's color image processor, because both have bit discarding in order to correct for the upper M bits in the N bits of a digital color image signal, given the express suggestion of Takaoka, (col. 1, lines 60-66).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Noda, JP 2000-228731, to reduce noise without losing image quality.

Peterson, US-PAT-NO: 6,598,197 B1, to conceal errors in digital data

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melanie M Vida whose telephone number is (703) 306-4220. The examiner can normally be reached on 8:30 am 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly A Williams can be reached on (703) 305-4863. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Melanie M Vida
Examiner
Art Unit 2626

MMV
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April 29, 2004

JEROME GRANT II
PRIMARY EXAMINER